PATENT
Attorney Docket No.: 8733D-6836

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
CHOI, Duck-Kyun	)	Art Unit: NOT ASSIGNED
Serial No:	)	Examiner: NOT ASSIGNED
Filed: October 13, 1998	)	
For: A METHOD FOR FABRICATING A THIN FILM TRANSISTOR	)	

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Dear Sir:

Transmitted herewith for filing is the patent application of
Inventor(s): **CHOI, Duck-Kyun of Seoul, Korea**
For: **A METHOD FOR FABRICATING A THIN FILM TRANSISTOR**

Enclosed are:
_X_ 12 Sheet(s) of drawings (_X_ informal)
_X_ An assignment of the invention to LG Electronics Inc. _X_ **WILL FOLLOW.**
__ An associate power of attorney.
_ A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.
_X_ Declaration and Power of Attorney. _X_ **WILL FOLLOW.**
_ Certified copy of Patent Application No. filed from which priority is claimed under 35 USC §119.
_X_ IDS enclosed. _X_ with references.
_ Preliminary Amendment

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	ITEM	NO. OF CLAIMS FILED MINUS BASE*		NO. OF CLAIMS OVER BASE	X SM/LG ENTITY FEE	$ AMOUNT	$ FEE
A	TOTAL CLAIMS FEE	24	- 20* =	4	X $11 or X $22	$88.00	
B	INDEPENDENT CLAIMS FEE**	2	- 3* =	0	X $41 or X 82	$0	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)						$88
D	MULTIPLE-DEPENDENT CLAIMS FEE				SMALL ENTITY FEE = $135 LARGE ENTITY FEE = $270		$
E	BASIC FEE*				SMALL ENTITY FEE = $395 LARGE ENTITY FEE = $790		$790.00
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)						$878
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Respectfully submitted,

Date: October 13, 1998

Jonathan Y. Kang
Reg. No. 38,199

LOEB & LOEB LLP
10100 Santa Monica Blvd., Suite 2200
Los Angeles, CA 90067-4164
Telephone: (310) 282-2000
Facsimile: (310) 282-2192

UNITED STATES PATENT APPLICATION

OF

DUCK KYUN CHOI

FOR

A METHOD FOR FABRICATING A THIN FILM TRANSISTOR

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a method of fabricating a thin film transistor, and more particularly, to a method of fabricating a thin film transistor by crystallizing an amorphous silicon layer into a polysilicon layer, thereby providing a polysilicon thin film transistor.

DISCUSSION OF THE RELATED ART

Recently, polysilicon (poly-Si) TFTs(Thin Film Transistors) have been actively investigated due to their potential in high mobility and current driving ability. They are usually applied to three-dimensional integrated circuits and active matrix liquid crystal displays (AMLCD). A low temperature process and short process times are essential for reducing the manufacturing cost. The use of relatively inexpensive glass substrates further reduces cost. However, most of the technologies adopt high temperature process for the crystallization of amorphous silicon. In poly-Si TFTs, the crystalline quality of silicon is of great importance since the integrated circuits are built with silicon film.

The effect of a small presence of metal impurities on the crystallization of amorphous silicon film was researched by Mayer

et al. Recently, one report has claimed that Ni can substantially decrease the crystallization temperature to as low as 480°C. It is proven that the nucleation and growth of crystalline silicon are mediated by the formation of nickel silicide($NiSi_2$) and the crystallization velocity is limited by the diffusion of $NiSi_2$ in MIC(MIC : Metal Induced Crystallization) method. MIC was further improved to MILC (Metal Induced Lateral Crystallization) where the crystalline seed($NiSi_2$) propagates into the metal-free area by thermal diffusion, thus obtaining large-grained poly-Si films with a small metal contamination.

Figs. 1A to Fig. 1B show a first example of fabricating a thin film transistor according to the related art. The following first example of the related art is from U.S. patent application serial number 08/833,131, which is owned by the same assignee as the present application and is hereby incorporated by reference, and "A Novel Self-Aligned Polycrystaline Silicon Thin-Film Transistor Using Silicide Layers" by Jai Il Ryu et. al., IEEE Electron Device Letters, Vol. 18, No. 6, June 1997.

Referring to Fig. 1A, a semiconductor layer 11 and a gate insulating film 13 are formed on an insulating substrate 10 in succession. Another semiconductor layer is formed on the gate

insulating film 13. The semiconductor layer on the gate insulating film 13 and the gate insulating film 13 are patterned together. Then, ion showering is performed to form heavily doped semiconductor layers 16 in the semiconductor layer on the gate insulating film 13 and the exposed semiconductor layer 11 on both sides of the gate insulating film 13.

Referring to Fig. 1B, nickel having a thickness of 30Å is RF-sputtered on the heavily doped semiconductor layer 16 to form a nickel silicide layer 12 over the gate insulating film 13 and both sides of the gate insulating film 13. In the sputtering method, a nickel target of 6N purity is preheated for 20 minutes at a temperature of 200°C under an initial vacuum of 3×10-6 Torr. The sputtering method is performed at 75W RF power for 5 seconds. Then, the substance is annealed in an argon ambient for one hour at a substrate temperature of 260°C to form nickel silicide layers 12. Residual nickel that did not react with silicon is removed by a mixture of HNO3 and HCl with a ratio of 1:5.

In the first example of the related art, as shown in Fig.2, the semiconductor layer 11 is used as an active layer of the thin film transistor, and the semiconductor layer 11 is formed by crystallizing amorphous silicon layer 11L into a polysilicon layer through laser annealing. Generally, laser crystallization

is performed by carrying out laser scanning on the amorphous silicon layer 11L on the substrate 10 for a long time, thereby crystallizing amorphous silicon layer into the polysilicon layer. As a result, the first example of the related art has the disadvantage of requiring a long process time. In addition, since this method gives a non-uniform crystallization, it is unsuitable for fabricating a plurality of transistors having uniform characteristics on the substrate.

Figs. 3A to Fig. 3D show a second example of fabricating a thin film transistor according to the related art. The following second example of the related art shows a method of fabricating a thin film transistor using the MILC technique.

Referring to Fig. 3A, an amorphous silicon layer is deposited on a substrate 30, and then the amorphous silicon layer is etched to form an active layer 31.

Referring to Fig. 3B, an oxide layer and an Mo layer are deposited on the active layer 31 and the substrate 30 in succession, and then, the Mo layer and the oxide layer are etched to form gate electrode 33 and gate insulating layer 32 on the active layer 31.

Referring to Fig. 3C, impurities having a first conductivity type are doped in the active layer formed by the amorphous

silicon layer to form a source region 31S and a drain region 31D in the active layer 31. Then, a nickel thin film 37 is deposited on the exposed and doped active layer.

Referring to Fig. 3D, a thermal treatment is performed on the resultant substrate comprising nickel thin film 37 at a temperature of about 500°C, to crystallize the amorphous silicon layer used as the active layer 31 into a polysilicon layer 31', thereby providing a polysilicon thin film transistor.

When performing the thermal treatment, a portion of the amorphous silicon layer that contacts the nickel thin film becomes nickel silicide 37'. The nickel silicide is used as a nucleus for crystallizing amorphous silicon into polysilicon. Silicon portions contacting nickel thin film 31, for example, the source region 31S and the drain region 31D, are crystallized by MIC, and a nickel-free region, for example, a channel region 31C, is crystallized by MILC. Here, a small amount of the nickel or nickel silicide contaminates the center of the channel region.

Therefore, the second example of the related art has the disadvantages of requiring long crystallization time and decreasing the characteristics of the thin film transistor due to contamination of the crystallized silicon layer by metal impurities, such as, nickel silicide.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a method for fabricating a thin film transistor that substantially obviates one or more of the problem due to limitations and disadvantages of the related art.

An object of the present invention is to provide a thin film transistor with high electric field mobility.

Another object of the present invention is to provide a thin film transistor with high on/off ratio with low leakage current.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, a method for fabricating a thin film transistor comprises the steps of forming an amorphous silicon layer as an active layer on a substrate; forming a gate insulating layer and a gate electrode on the amorphous silicon layer; doping impurities of first

conductive type in exposed portions of the amorphous silicon layer; forming metal layers on the doped portions of the amorphous silicon layer; crystallizing the amorphous silicon layer by performing heat treatment and applying electric field in the resultant substrate.

In another aspect of the present invention, a method for fabricating thin film transistor comprises the steps of forming a first amorphous silicon layer as an active layer on a substrate; forming a gate insulating layer and a second amorphous silicon layer as a gate electrode on the first amorphous silicon layer; doping impurities of first conductive type at exposed portions of the first and second amorphous silicon layers; forming metal layers on the doped portions of the first and second amorphous silicon layers; crystallizing the first and second amorphous silicon layers by performing heat treatment and applying electric field in the resultant substrate.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of the specification, illustrates embodiments of the invention and together with description serve to explain the principles of the invention.

In the drawings:

Fig. 1A to Fig. 1B show a process of fabricating a thin film transistor according to a first example of the related art;

Fig. 2 shows a laser annealing technique for crystallizing an amorphous silicon layer according to the first example of the related art;

Fig. 3A to Fig. 3D show a process of fabricating a thin film transistor according to a second example of the related art;

Fig. 4A to Fig. 4E show a process of fabricating a thin film transistor according to a first embodiment of the present invention;

Fig. 5 shows metal induced lateral crystallization (MILC) and field aided lateral crystallization (FALC);

Fig. 6 shows a threshold voltage of the thin film transistor according to the first embodiment of the present invention;

Fig. 7 shows transfer characteristics of the thin film transistor according to the first embodiment of the present invention;

Fig. 8A to Fig. 8E show a process of fabricating a thin film transistor according to a second embodiment of the present invention;

Fig. 9 shows a threshold voltage of the thin film transistor according to the second embodiment of the present invention; and

Fig. 10 shows transfer characteristics of the thin film transistor according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Fig. 4A to Fig. 4E show a process of fabricating a thin film transistor according to a first embodiment of the present invention.

Referring to Fig. 4A, an amorphous silicon layer is deposited on a substrate 400, and then, the amorphous silicon layer is etched by photolithography to form an active layer 41. The amorphous silicon layer of 1000Å thickness is deposited on

the substrate 400 by PECVD at 300°C using Si2H6. The active layer 41 is etched by photolithography by RIE system using SF6 gas.

The substrate 400 is prepared using glass substrate itself. The substrate 400 can also be prepared by depositing an oxide layer 410 of 5000Å thickness on a silicon wafer having a first conductivity type, such as p-type silicon wafer.

Referring to Fig. 4B, an oxide layer and an Mo layer is deposited on the active layer and the substrate in succession, and then, the Mo layer and the oxide layer are etched by photolithography in succession to form a gate electrode 43 and a gate insulating layer 42.

An oxide layer of 1000Å thickness is deposited by RF sputtering from an SiO2 target in a 25% oxygen - 75% argon mixture at temperature of 200°C and an Mo layer of 3500Å thickness is deposited by sputtering at room temperature. Then, the Mo layer is etched by photolithography using a mask for forming a gate pattern to form the gate electrode 43. The oxide layer is etched to form the gate insulating layer 42.

Referring to Fig. 4C, impurities having a first conductivity type are doped in the active layer 41 to form a source region 41S

and a drain region 41D in the active layer 41. Then, nickel thin film 45 is deposited on the exposed and doped active layer.

Ion mass doping using PH3 is performed at exposed portions of the resultant substrate at room temperature, and then, nickel thin film of no more than 30Å thickness is formed on the doped silicon layer of the active layer 41. Here, the step of forming metal layers on the doped portions of the amorphous silicon layer may be performed before the step of doping impurities in exposed portions of the amorphous silicon layer. Here, the nickel thin film layer could be replaced with metal thin film formed by transition metal material comprising Pd, Co, Cu, Cr, Au, Fe or Ti

Referring to Fig. 4D, thermal treatment and electric field are applied to the resultant substrate comprising nickel thin film 45.

Electrodes 47 such as Au were formed on the resultant substrate and voltage is applied to the Au electrodes during the thermal treatment in N_2 ambient.

Referring to Fig. 4E, as a result of applying electric field and thermal treatment at a temperature below 500°C, the amorphous silicon layer is crystallized into polysilicon layer 41', thereby providing polysilicon thin film transistor. Here, the Au

electrodes could be replaced with metal electrodes formed by conventional metal material including Pt, Fe or Al.

When performing thermal treatment, a portion of the amorphous silicon layer that contacts the nickel thin film becomes nickel silicide 45'. A portion of the nickel silicide is used as a nucleus for crystallizing amorphous silicon into polysilicon. Silicon portions contacting nickel thin film 41, for example, the source region 41'S and the drain region 41'D, are crystallized by MIC, and the nickel-free regions, for example, the channel region 41'C, are crystallized by crystallization of FALC (Field Aided Lateral Crystallization). The nickel on the surface of the substrate is volatilized during thermal treatment. The nickel on the gate electrode is either volatilized or remains. In case the nickel remains on the gate electrode, the nickel is used as the gate electrode also.

The crystallization rate of FALC is much faster than that of the crystallization method of the related arts. FALC shows the directionality in crystallization velocity at the negative electrode is faster than that at the positive electrode. This lateral crystallization is rapidly performed at the negative (-) electrode relative to the positive (+) electrode due to the effect of the applied electric field. As a consequence, it is

possible to accelerate the unidirectional crystallization of silicon with the application of the electric field. In FALC, NiSi2 phase is driven by the electric field. It is believed that the advancing growth front sweeps across the channel region and stops at either of the source and drain region depending on the polarity. Therefore, there is no metal contamination in the channel region in the thin film transistor fabricated according to the present invention.

When performing thermal treatment, the doped impurities in the active layer undergo activation.

The present invention uses the technique of forming the electric field for crystallizing the amorphous silicon layer during thermal treatment of the resultant substrate.

Fig. 5A and Fig. 5B show two specimens crystallized by conventional MILC technique (as described in the second example of the related art) and FALC technique according to the present invention (as described in the first embodiment of the present invention) at an identical condition, at a temperature of 500°C and at 2 hours, respectively. The only difference was the application of an electric field of 11.8 V/cm to the specimen crystallized by FALC technique.

Referring to Fig. 5A which shows MILC, crystallization starts at the source and drain region of the transistor and propagates from both sides to the center of the channel. Therefore, its leading edge($NiSi_2$) ends up midway between the source and drain (center of the gate). The crystallization in the channel region was not complete even after 2 hours had elapsed. The crystallization rate was 8 μm/h. It is believed that the metallic phases at the center of the channel deteriorate the electrical properties of the poly-silicon TFTs.

Referring to Fig. 5B which shows FALC, on the other hand, with the aid of an electric field of 11.8V/cm, for example, and under the same crystallization conditions, the complete directional crystallization of polarity dependence is shown from the negative electrode to the positive electrode. The crystallization in the channel region was completed within 2 hours time. The crystallization rate was 55μm/h and the metallic contamination was swept out of the channel region.

Fig. 6 shows the threshold voltage of 2.1V for the FALC poly-silicon TFT fabricated according to the first embodiment of the present invention.

Fig. 7 shows the transfer characteristics of the FALC poly-silicon TFT fabricated according to the first embodiment of the present invention.

A summary of the TFTs performance parameters is given in Table 1.

Table. 1

	MILC TFT (500°C, 10h)	FALC TFT (500°C, 10h, E=4 V/cm)
L/W (μm)	15/15	15/15
Mobility (cm2/Vs)	22.65	56.74
vth (V)	2.6	2.1
on/off ratio	3.09×106	2.89×107
Off current (A)	1.31×10-12	3.72×10-13

As shown in Fig. 6, Fig. 7 and Table 1, the transfer characteristics for the FALC TFT as well as the conventional MILC TFT is well behaved in general. For off-current(leakage-current) characteristics, a noticeably low off current of 3.72×10-13A is shown, which means lower power consumption.

Fig. 8A to Fig. 8E show a process of fabricating a thin film transistor according to a second embodiment of the present invention.

Referring to Fig. 8A, a first amorphous silicon layer for forming the active layer is formed on a substrate 800.

An amorphous silicon layer of 1000Å thickness is deposited on the substrate 800 by Low Pressure Chemical Vapor Deposition (LPCVD) at 480°C using Si2H6, for example, and then is etched by photolithography to form the first amorphous silicon layer 81 as the active layer by an RIE system using SF6 gas and by using a mask for an active pattern.

The substrate 800 is prepared using glass substrate itself. The substrate 800 may be prepared by depositing an oxide layer 810 of 5000Å thick on silicon wafer having a first conductivity type, such as a p-type silicon wafer.

Referring to Fig. 8B, a gate insulating layer 82 and a second amorphous silicon layer for forming a gate electrode are formed on the first amorphous silicon layer 81.

An oxide layer of 1000Å thickness is deposited by RF sputtering from an SiO2 target in a 20% oxygen - 80% argon mixture and another amorphous silicon layer of 1000Å thick is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) at a temperature of 300°C. Then, the amorphous silicon layer is etched by photolithography using a mask for gate patterning to

form gate electrode 83. The oxide layer is etched to form gate insulating layer 82.

Referring to Fig. 8C, impurities having a first conductivity type are doped at exposed portions of the first and second amorphous silicon layers 81 and 83. Then, nickel thin film 87 is formed on the exposed and doped silicon layers. As a result of doping, a source region and a drain region 81D are formed in the first amorphous silicon layer 81.

Ion doping using 3% B2H6 is performed in exposed portions of the resultant substrate at room temperature. Then, nickel thin film of no more than 30Å thickness is formed on the doped silicon layers 81 and 83. Here, the step of forming metal layers on the doped portions of the amorphous silicon layers can be performed before the step of doping impurities in exposed portions of the amorphous silicon layers. The nickel thin film layer may be replaced with a metal thin film formed by one or more of the transition metal material including Cu, Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Se, Ti, V, Cr, Mn, Zn, Au and Ag. Additional transition metal materials may be found in USP 5,605,846 and USP 5,654,203, for example.

Referring to Fig. 8D, thermal treatment and electric field are applied to the resultant substrate comprising nickel thin film 87.

Electrodes 89 such as Au are formed on the resultant substrate and electric field is applied simultaneously with thermal treatment. Here, the Au electrodes may be replaced with metal electrodes formed by conventional metal material including Pt, Fe or Al.

As a result of applying the electric field and thermal treatment at a temperature below 500°C, the amorphous silicon layer is crystallized into polysilicon layer 81', thereby providing a polysilicon thin film transistor.

When performing thermal treatment, a portion of the amorphous silicon layer that contacts the nickel thin film becomes nickel silicide 87'. A portion of the nickel silicide is used as a nucleus for crystallizing amorphous silicon into polysilicon. Silicon portions contacting nickel thin film 81, for example, the source region 81'S and the drain region 81'D are crystallized by MIC, and the nickel-free region, for example, the channel region 81'C, is crystallized by FALC.

The nickel on the surface of the substrate is volatilized during thermal treatment. The nickel on the gate electrode is either volatilized or remains.

The crystallization rate of FALC is much faster than that of the crystallization method of the related arts. FALC shows the directionality in crystallization rate at the negative electrode is faster than that at the positive electrode. In FALC, NiSi2 phase is driven by the electric field. It seems that the advancing growth front will sweep across the channel region and stop at either the source or drain region depending on the polarity. Therefore, there is no metal contamination in the channel region in the thin film transistor fabricated according to the present invention.

When performing thermal treatment, the doped impurities in the active layer undergo activation.

Fig. 9 shows the threshold voltage of -7.4 V for the FALC poly-silicon TFT fabricated according to the second embodiment of the present invention.

Fig. 10 shows the transfer characteristics of the FALC poly-silicon TFT fabricated according to the second embodiment of the present invention.

A summary of the TFTs performance parameters is given in Table 2.

Table. 2

	The conventional MILC TFT (600° C., 24h)	FALC TFT (500°C, 80min, E=4 V/cm)
L/W (μm)	10/10	8/20
Mobility (cm2/Vs)	15.7	23
Vth (V)	13	-7.3
on/off ratio	1.37×106	6.5×105 (Vd=-0.1V)
Off current (A)	2.1×10-10	6.5×10-11

As shown in Fig. 9, Fig. 10 and Table 2, the characteristics for the FALC devices as well as the conventional TFTs devices were well behaved in general. In off-current (leakage-current) characteristics, a noticeably low off current of 3.72×10-13A was shown, which means lower power consumption.

The present invention provides a thin film transistor with good physical characteristics such as high electric field mobility, high on/off ratio, and low leakage current by fabricating thin film transistors in a short process time through the electric field and thermal treatment.

Thin film transistors according to the present invention has been successfully fabricated in an amorphous silicon layer using FALC instead of conventional MILC in order to get high-performance. The conventional crystallization temperature of amorphous silicon layer is at least 600°C, the present technique is attractive because it can lower the process temperature below 500°C and reduce the process time.

The FALC demonstrated polarity dependence of directional crystallization, which leads to non-contaminated single grained channel. Hence, the novel technique, FALC, will enable the use of glass substrates for the poly-Si TFT application. Moreover FALC has also proven its superiority in quality of the devices.

The present invention is used in fabricating thin film transistors of the first and second embodiments, and thin film transistors having offset or LDD structure.

It will be apparent to those skilled in the art that various modifications can be made in the method of fabricating a thin film transistor of the present invention without departing from the sprit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method of fabricating a thin film transistor comprising the steps of:

forming an amorphous silicon layer as an active layer on a substrate;

forming a gate insulating layer and a gate electrode on the amorphous silicon layer;

doping impurities of a first conductive type in the amorphous silicon layer;

forming a metal layer on the exposed portions of the amorphous silicon layer; and

crystallizing the amorphous silicon layer by applying thermal treatment and electric field to the resultant substrate.

2. The method of fabricating a thin film transistor according to claim 1, wherein the substrate includes one of a glass and an oxide layer on a glass.

3. The method of fabricating a thin film transistor according to claim 1, wherein the substrate is prepared by depositing a silicon wafer or an oxide layer on a silicon wafer.

4. The method of fabricating a thin film transistor according to claim 1, wherein the gate electrode is formed by at least one transition metal material including Mo, Cr and Co.

5. The method of fabricating a thin film transistor according to claim 1, wherein the impurities include PH3.

6. The method of fabricating a thin film transistor according to claim 1, wherein the metal layer has a thickness of no more than 30Å.

7. The method of fabricating a thin film transistor according to claim 6, wherein the metal layer is formed by at least one transition metal material including Cu, Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Se, Ti, V, Cr, Mn, Zn, Au and Ag.

8. The method of fabricating a thin film transistor according to claim 1, wherein the step of forming metal layers on the doped portions of the amorphous silicon layer is performed before the step of doping impurities of first conductive type in exposed portions of the amorphous silicon layer.

9. The method of fabricating a thin film transistor according to claim 1, further comprising a step of forming electrodes for applying a voltage to form the electric field on the resultant substrate.

10. The method of fabricating a thin film transistor according to claim 9, wherein the electrodes are formed by a metal material including Au, Pt, Fe and Al.

11. The method of fabricating a thin film transistor according to claim 9, wherein the electrodes includes first and second electrodes, and crystallization of the amorphous silicon layer occurs faster at the first electrode than at the second electrode.

12. The method of fabricating a thin film transistor according to claim 9, wherein the electrodes includes a negative electrode and a positive electrode, and crystallization of the amorphous silicon layer occurs faster at the negative electrode than at the positive electrode.

13. The method of fabricating a thin film transistor according to claim 1, wherein the heat treatment is performed at about 500°C.

14. A method of fabricating a thin film transistor comprising the steps of:

forming a first amorphous silicon layer as an active layer on a substrate;

forming a gate insulating layer and a second amorphous silicon layer as a gate electrode on the first amorphous silicon layer;

doping impurities of a first conductive type in the first and second amorphous silicon layers;

forming a metal layer on the doped portions of the first and second amorphous silicon layers; and

crystallizing the first and second amorphous silicon layers by performing heat treatment and applying electric field on the resultant substrate.

15. The method of fabricating a thin film transistor according to claim 14, wherein the substrate includes one of a glass and an oxide layer on a glass.

16. The method of fabricating a thin film transistor according to claim 14, wherein the substrate is prepared by depositing an oxide layer on a silicon wafer.

17. The method of fabricating a thin film transistor according to claim 14, wherein the step of forming the gate insulating layer and the second amorphous silicon layer comprises the steps of:

depositing an oxide layer and an amorphous silicon layer on the substrate comprising the first amorphous silicon layer;

etching the oxide layer and the amorphous silicon layer using a mask for forming the gate electrode.

18. The method of fabricating a thin film transistor according to claim 14, wherein the impurities include p-type or n-type.

19. The method of fabricating a thin film transistor according to claim 14, wherein the metal layer has a thickness of no more than 30Å.

20. The method of fabricating a thin film transistor according to claim 14, the step of forming metal layers on the doped portions of the amorphous silicon layer is performed before the step of doping impurities of first conductive type in exposed portions of the first and second amorphous silicon layers.

21. The method of fabricating a thin film transistor according to claim 14, further comprising a step of forming electrodes for is applying a voltage to form the electric field on the resultant substrate.

22. The method of fabricating a thin film transistor according to claim 21, wherein the electrodes are formed by a metal material including Au, Pt, Fe and Al.

23. The method of fabricating a thin film transistor according to claim 21, wherein the electrodes includes first and second electrodes, and crystallization of the amorphous silicon layer occurs faster at the first electrode than at the second electrode.

24. The method of fabricating a thin film transistor according to claim 21, wherein the electrodes includes a negative electrode and a positive electrode, and crystallization of the amorphous silicon layer occurs faster at the negative electrode than at the positive electrode.

ABSTRACT OF THE DISCLOSURE

A method of fabricating a thin film transistor includes forming an amorphous silicon layer as an active layer on a substrate, forming a gate insulating layer and a gate electrode on the amorphous silicon layer, doping impurities of a first conductive type in the amorphous silicon layer, forming a metal layer on the exposed portions of the amorphous silicon layer, and crystallizing the amorphous silicon layer by applying thermal treatment and electric field to the resultant substrate.

FIG .1A

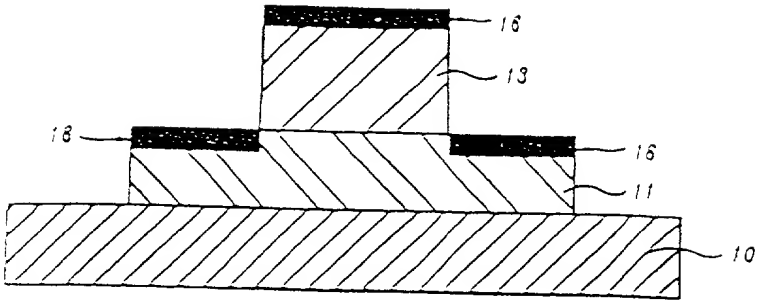


FIG .1B

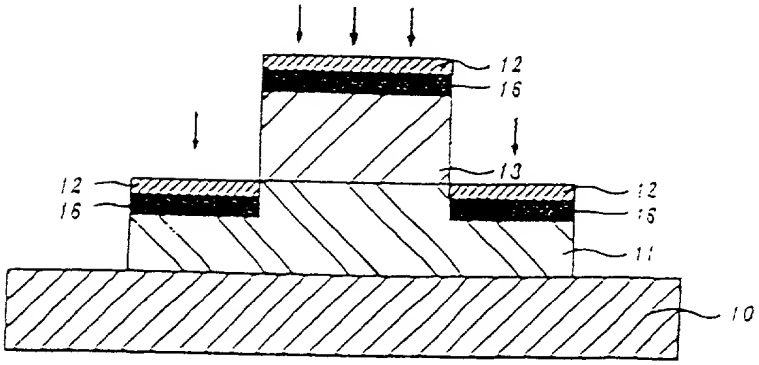


FIG .2

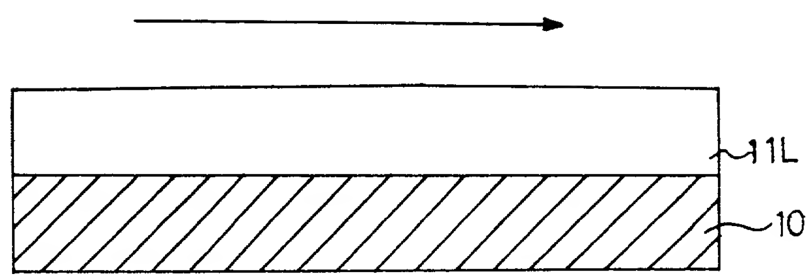


FIG .3A

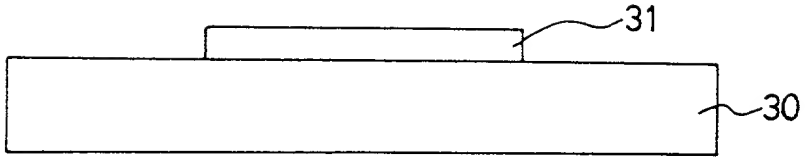


FIG .3B

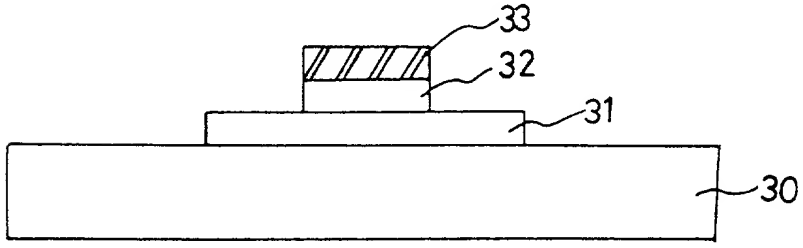


FIG .3C

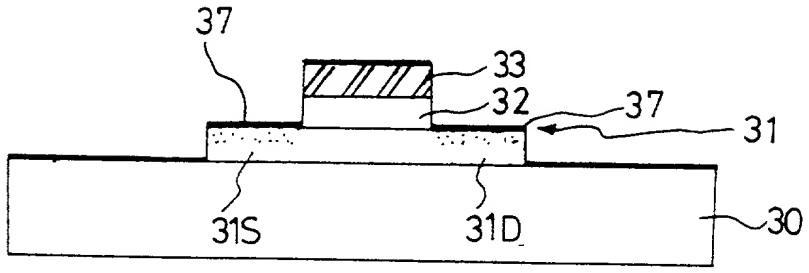


FIG .3D

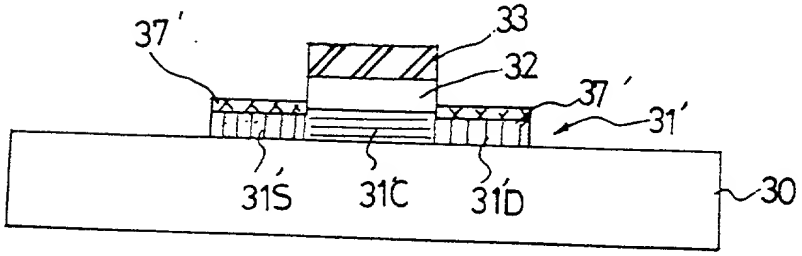


FIG .4A

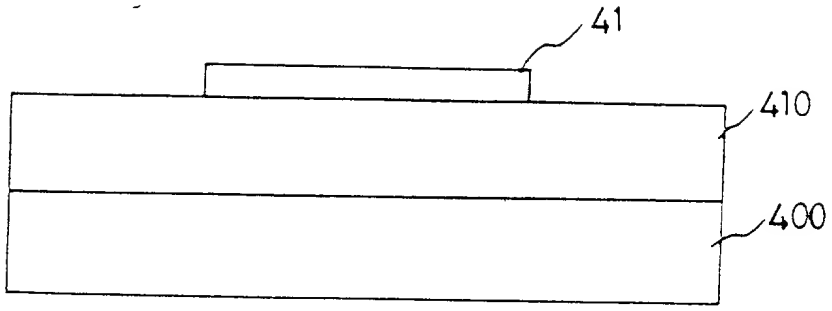


FIG .4B

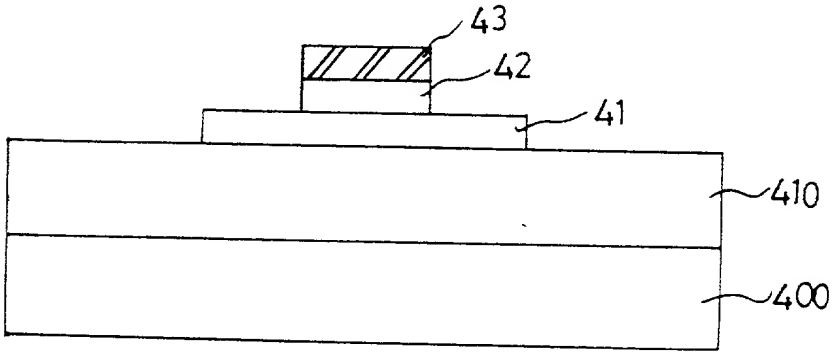


FIG .4C

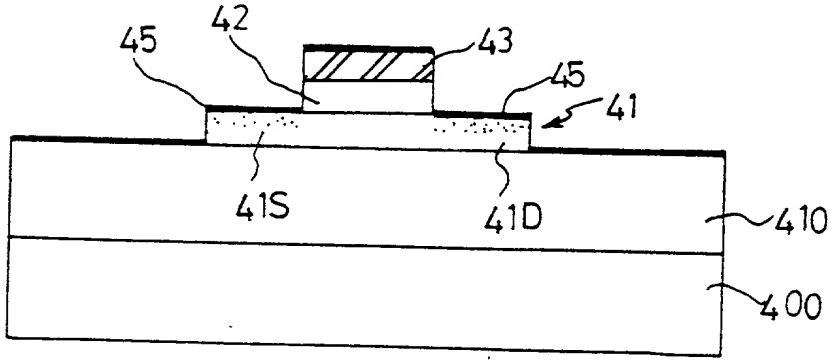


FIG .4D

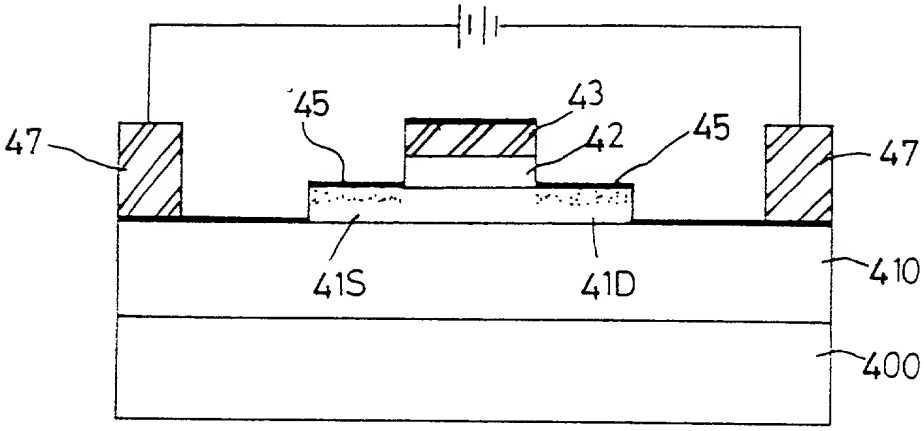


FIG .4E

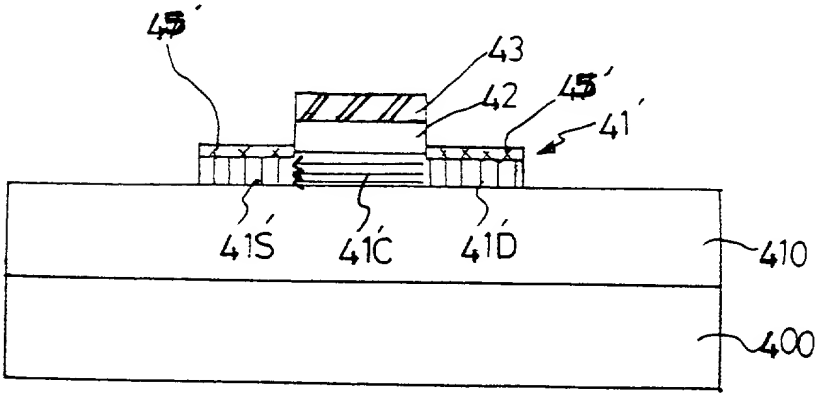


FIG. 5

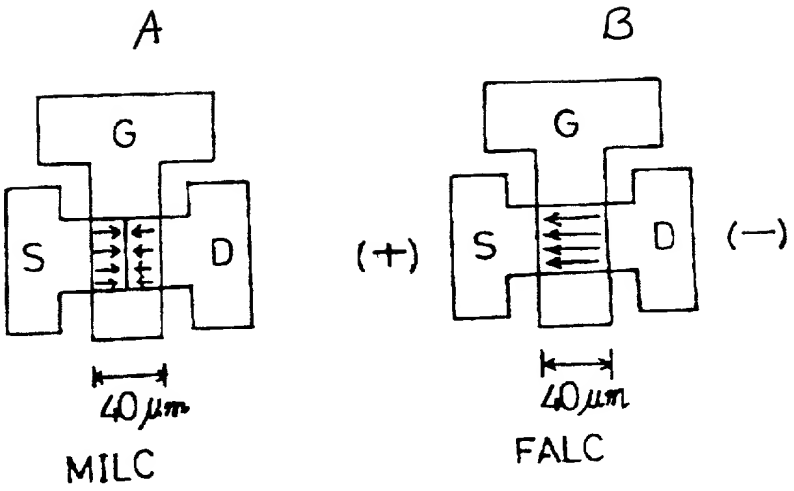


FIG .6

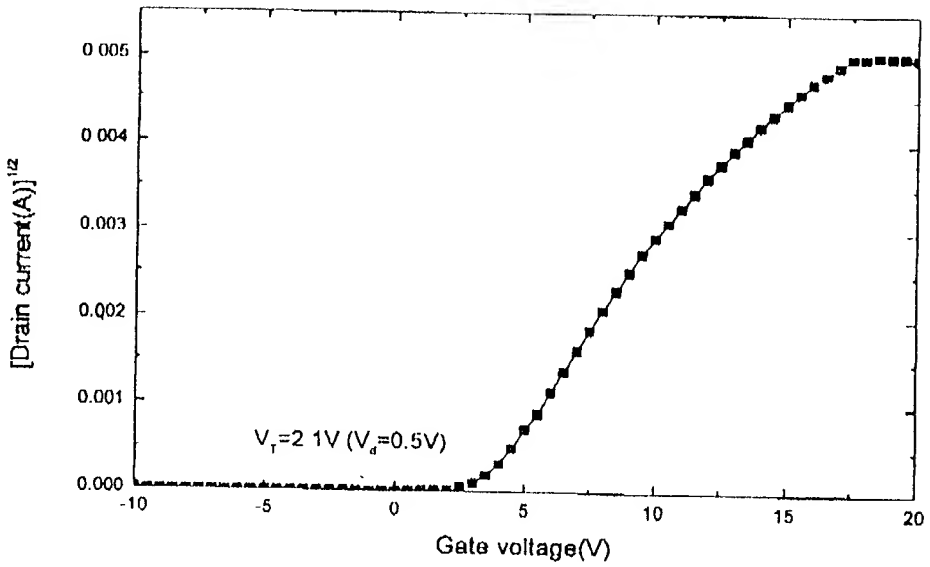


FIG .7

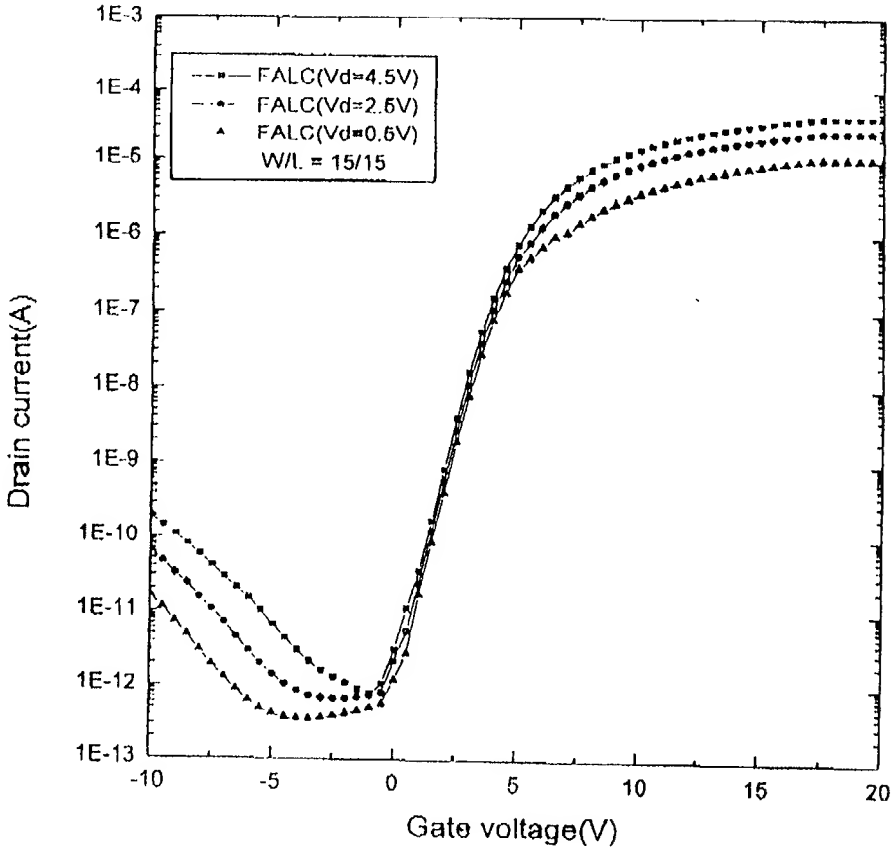


FIG .8A

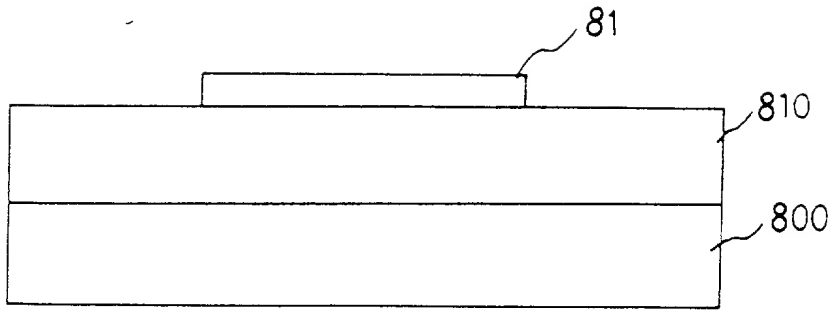


FIG .8B

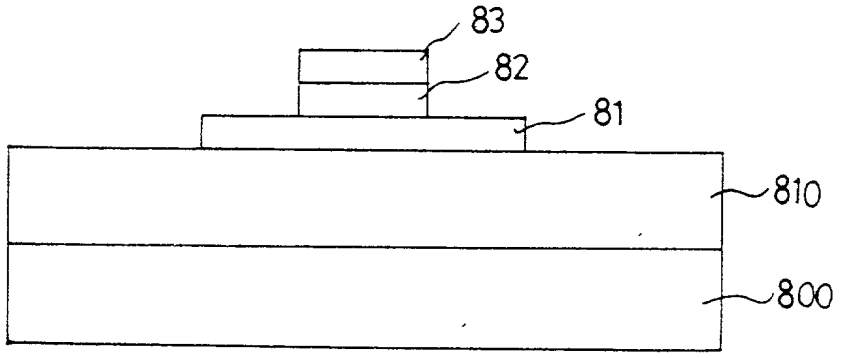


FIG .8C

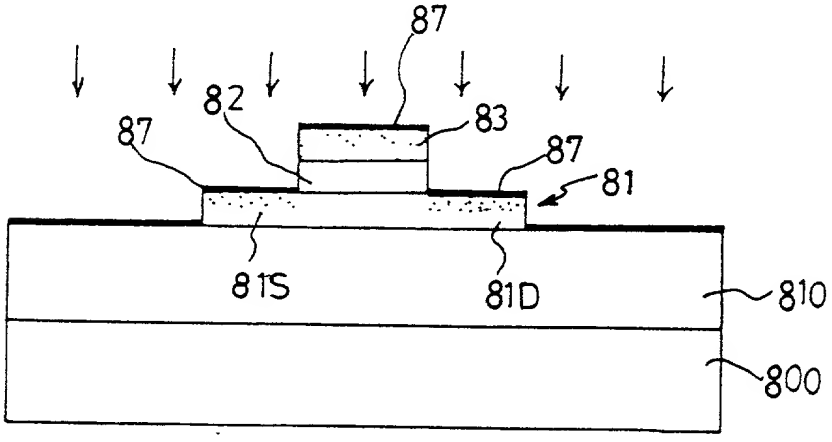


FIG .8D

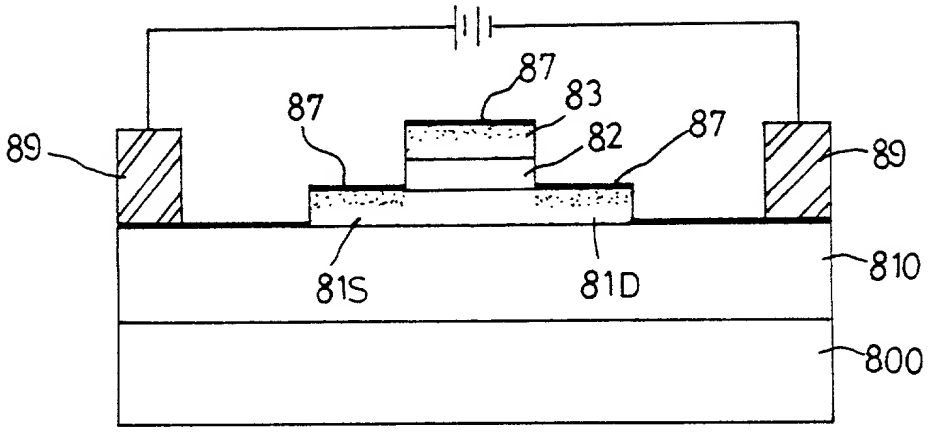

87
83
87
82
87
89
89
810
81S
81D
800

FIG .8E

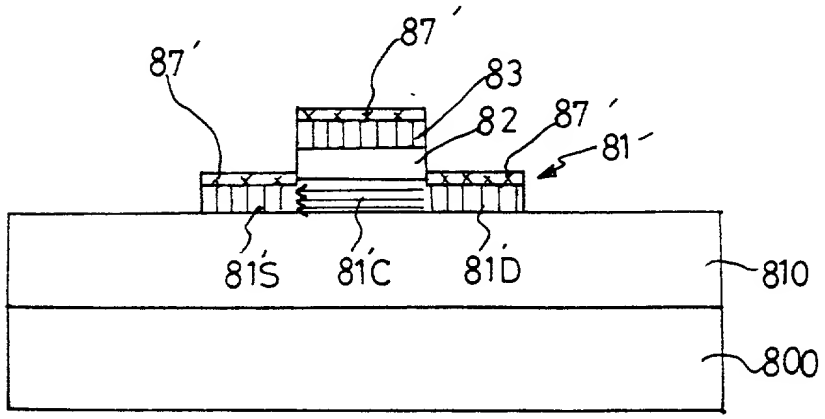

87'
87'
83
82
87'
81'
810
81'S
81'C
81'D
800

FIG .9

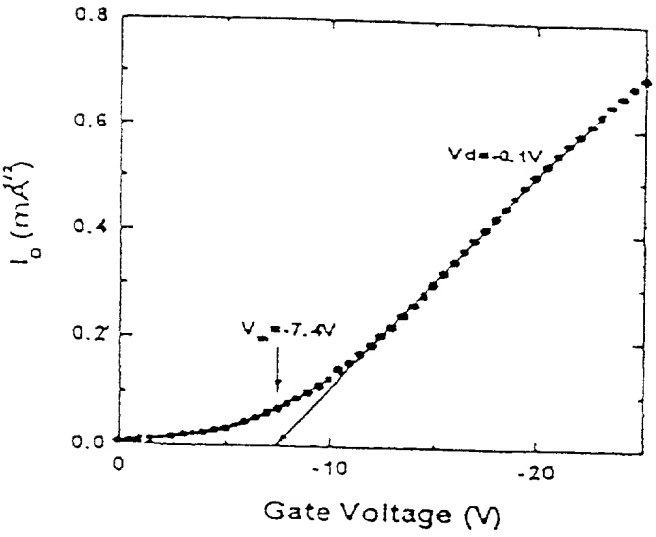
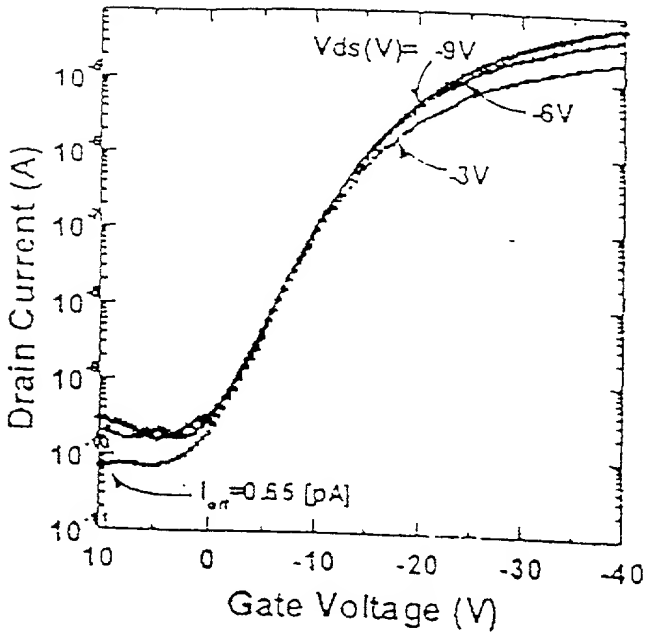

0.8
0.6
0.4
0.2
0.0
I_D (mA$^{1/2}$)
Vd=-0.1V
V_{th}=-7.4V
0
-10
-20
Gate Voltage (V)

FIG .10


Vds(V)= -9V
-6V
-3V
I_{off}=0.55 [pA]
Drain Current (A)
10
0
-10
-20
-30
-40
Gate Voltage (V)